## Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

## Listing of Claims:

Claim 1.    (Currently Amended):  A signal processing circuit for processing an input digital video signal and producing display data for a display unit divided into a plurality of regions to be driven, comprising:

a data separation portion for performing assignment of said input digital video data; and

a plurality of memory portions for storing said the digital data which is digital video data assigned by said data separation portion; each of said memory portions including an input-side line memory having a data storage capacity equal to or greater than the number of pixels of said display unit in a horizontal direction divided by the number of said regions and sequentially receiving and storing said digital data, and an output-side line memory for holding the serial data stored in said input-side line memory and transferred in parallel from said input-side line memory and having a plurality of output portions capable of serially outputting the data held therein from prescribed positions different from each other; wherein

selection is made among said plurality of output portions of said output-side line memory in accordance with the number of pixels of said display unit in a horizontal direction, and serial output data is supplied from the selected output portion in each of said plurality of memory portions to said display unit as analog display data.

Claim 2.    (Original):  The signal processing circuit recited in claim 1, wherein the number of said plurality of memory portions provided in said circuit is

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determined corresponding to the number of regions into which said display unit is divided in a horizontal direction.

Claim 3.    (Original):    The signal processing circuit recited in claim 1, wherein

said input-side line memory is an n-stage input side shift register for sequentially holding said digital data received at a data input terminal of a first stage, the number n being equal to or greater than the number of pixels of said display unit in a horizontal direction divided by the number of said regions, and

said output-side line memory includes

an n-stage output side shift register having the same number of stages as said input side shift register, and

an input data switch circuit for switching, as input data for each stage of said n-stage output side shift register, output data which can be transferred in parallel from each stage of said n-stage input side shift register, and output data shifted from an immediately preceding or succeeding stage of said n-stage output side shift register.

Claim 4.    (Original):    The signal processing circuit recited in claim 3, wherein said plurality of output portions are each uniquely connected to a data output in a predetermined and different stage of said n-stage output side shift register.

Claim 5.    (Original):    The signal processing circuit recited in claim 1, wherein the data storage capacities of said input-side line memory and of said output-side line memory correspond to 400 pixels or 512 pixels.

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Claim 6.    (Previously Presented):  The signal processing circuit recited in claim 1, wherein said plurality of output portions of said output-side line memory can output serial data in a sequential manner starting from a 400$^{th}$, a 320$^{th}$, and a 256$^{th}$ data item counting from a last input data item of said digital data serially input to said input-side line memory.

Claim 7.    (Original):  The signal processing circuit recited in claim 6, wherein one of said plurality of output portions of said output-side line memory outputs the data in a serial manner starting from the last input data item of said digital data serially input to said input-side line memory.

Claim 8.    (Original):  The signal processing circuit recited in claim 1, wherein

the number of said plurality of memory portions is equal to the product of the number of regions into which said display unit is divided in a horizontal direction and the number of primary colors displayed at said display unit, and

said memory portions respectively receive said digital video signals corresponding to the regions and/or primary colors different from each other.

Claim 9.    (Original):  The signal processing circuit recited in claim 1, wherein

said input digital video signal is input every horizontal scanning period, and

parallel data transfer from said input-side line memory to said output-side line memory is performed during a horizontal blanking period.

Claim 10.    (Currently Amended):  A signal processing circuit for processing an input digital video signal and producing display data for a display unit divided into a plurality of regions to be driven, comprising:

a data separation portion for performing assignment of said input digital video data;

a plurality of memory portions for storing ~~said~~ the digital data which is digital video data assigned by said data separation portion; each of said memory portions including an input-side line memory having a data storage capacity equal to or greater than the number of pixels of said display unit in a horizontal direction divided by the number of said regions and sequentially receiving and storing said digital data, and an output-side line memory for holding the serial data stored in said input-side line memory and transferred in parallel from said input-side line memory and having a plurality of output portions capable of serially outputting the data held therein from prescribed positions different from each other; and

an output selector for selecting among said plurality of output portions of said output-side line memory in accordance with the number of pixels of said display unit in a horizontal direction; wherein

the serial output data supplied from each of said plurality of memory portions through said output selector is converted into analog data and the converted data is supplied to said display unit as display data by a digital-analog conversion processing portion.

Claim 11.    (Original):   The signal processing circuit recited in claim 10, wherein

said input-side line memory is an n-stage input side memory for sequentially holding said digital data received at a data input terminal of a first stage, the number n being equal to or greater than the number of pixels of said display unit in a horizontal direction divided by the number of said regions, and

said output-side line memory includes

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an n-stage output side memory having the same number of stages as said input side memory, and

an input data switch circuit for switching, as input data for each stage of said n-stage output side memory, output data which can be transferred in parallel from each stage of said n-stage input side memory, and output data shifted from an immediately preceding or succeeding stage of said n-stage output side memory.

Claim 12.    (Original):   The signal processing circuit recited in claim 11, wherein said output-side line memory further includes a shift direction switch circuit for switching a data shift direction in said n-stage output side memory to an m-1 (where m<n) stage direction or an m+1 stage direction.

Claim 13.    (Original):   The signal processing circuit recited in claim 12, wherein said plurality of output portions of said output-side line memory at least include the output portion connected to a data output of the first stage of said n-stage output side memory and the output portion connected to the data output of k stage, where 1<k≤n.

Claim 14.    (Original):   The signal processing circuit recited in claim 13, wherein

in one of said plurality of memory portions, the output portion connected to the data output of said k stage is selected among said plurality of output portions of said output side memory, and data is read out from said output side memory following the order in which data is input to said input side memory, and

in the other of said plurality of memory portions, the output portion connected to the data output of said first stage is selected among the plurality of

output portions, and data is read out from said output side memory in the reverse order from which data is input to said input side memory.

Claim 15.   (Original):  The signal processing circuit recited in claim 14, wherein the data items stored in said plurality of memory portions are the digital video signals corresponding to adjacent regions of said display unit.

Claim 16.   (Original):  The signal processing circuit recited in claim 14, wherein, when a mirror image signal is input to said output selector, said output selector selects the output portion connected to the data output of the k stage among the plurality of output portions of said output side memory for said one of said plurality of memory portions, and selects the output portion connected to the data output of the first stage among said plurality of output portions for said other of said plurality of memory portions.

Claim 17.   (Original):  The signal processing circuit recited in claim 13, wherein the numbers n and k are any of 512, 400, 320, and 256.

Claim 18.   (Original):  The signal processing circuit recited in claim 13, wherein

the number of said plurality of memory portions is equal to the product of the number of regions into which said display unit is divided in a horizontal direction and the number of primary colors displayed at said display unit, and

said memory portions respectively receive said digital video signals corresponding to the regions and/or primary colors different from each other.

Claim 19.   (Original):  The signal processing circuit recited in claim 10, wherein

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said input digital video signal is input every horizontal scanning period, and

parallel data transfer from said input-side line memory to said output-side

line memory is performed during a horizontal blanking period.

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